CLAIMS

What is claimed is:

1. A semiconductor package with a heat dissipating structure, comprising:

a substrate;

at least a chip mounted on the substrate and electrically connected to the substrate via a plurality of conductive elements;

a heat dissipating structure comprising a flat portion, and a plurality of support portions formed at edges of the flat portion for supporting the flat portion in position above the chip, wherein the support portions are mounted at predetermined area on the substrate to be free of interference with arrangement of the chip and the conductive elements, and the support portions are arranged to form a space embraced by adjacent support portions and the flat portion, which space is dimensioned to accommodate the conductive elements and to allow the conductive elements to pass through the space to reach area on the substrate outside coverage of the heat dissipating structure; and

an encapsulant formed on the substrate for encapsulating the chip and the conductive elements.

2. The semiconductor package of claim 1, further comprising:

a plurality of solder balls implanted on the substrate and exposed to outside of the encapsulant.

3. The semiconductor package of claim 1, wherein the conductive elements are bonding wires, and a plurality of bond fingers are formed on the substrate for allowing the bonding wires to be bonded to the bond fingers.

4. The semiconductor package of claim 3, wherein the flat portion is elevated above the chip by the support portions and forms a predetermined height difference with respect to the substrate, allowing the height difference to be at least corresponding to height of

wire loops of the bonding wires.

5. The semiconductor package of claim 4, wherein part of the bond fingers are situated on the substrate at area outside the coverage of the heat dissipating structure, allowing the corresponding bonding wires to pass through the space embraced by adjacent support portions and the flat portion and to reach the outside-coverage bond fingers.

6. The semiconductor package of claim 1, wherein the support portions are situated at edge corners of the flat portion.

7. The semiconductor package of claim 1, wherein the flat portion has a top surface exposed to outside of the encapsulant, and a bottom surface opposed to the top surface, the bottom surface being formed with the support portions.

8. The semiconductor package of claim 7, wherein at least a protrusion is formed on the bottom surface of the flat portion and extends toward the chip.

9. The semiconductor package of claim 7, wherein at least a peripherally-situated recess is formed on the top surface of the flat portion.

10. The semiconductor package of claim 1, wherein each of the support portions is formed with at least a hole for allowing an encapsulating resin used for forming the encapsulant to pass through the hole.

11. The semiconductor package of claim 1, wherein each of the support portions is formed with a contact portion at a position in contact with the substrate.

12. The semiconductor package of claim 11, wherein the contact portion substantially extends laterally with respect to the substrate.

13. The semiconductor package of claim 11, wherein the contact portion is of a triangular shape.

14. The semiconductor package of claim 11, wherein the contact portion is of a rectangular shape.

15. The semiconductor package of claim 11, wherein the contact portion is of a semicircular shape.